

**Cairo University**

**Faculty of Engineering**

**Electronics and Electrical Communications Engineering Department**

**Course Code ELC2060**

**Course Title Electronic circuits**

**Electronics project**

**Under supervision of : Eng. Bassem Abd el-Aziz**

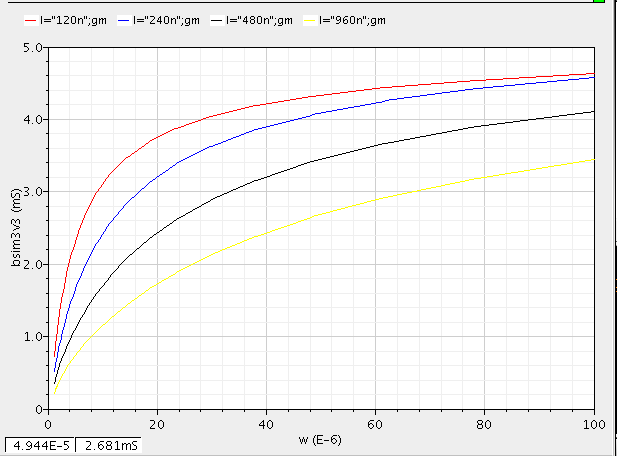
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| Name | Section | B.N |
| Khaled Ahmed | 2 | 5 |
| Khaled Khalifa | 2 | 7 |

# Task 1:

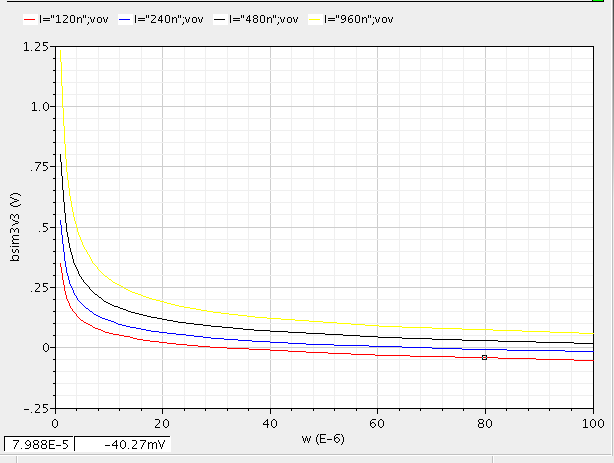
# The characteristics graphs for the N\_12\_HS\_L130E at bias current .

Figure 1:The characteristics graphs

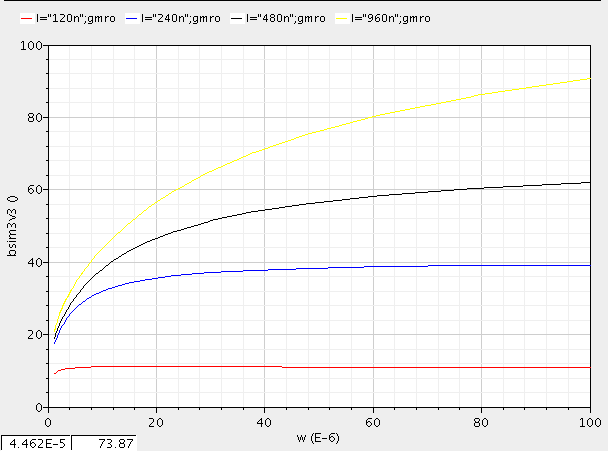
The long channel equation for each of the above simulated parameters:

1. gm

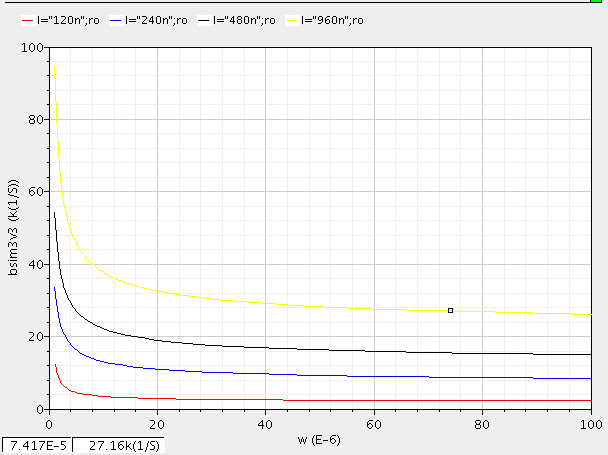
Which is similar to the obtained results in the simulation.



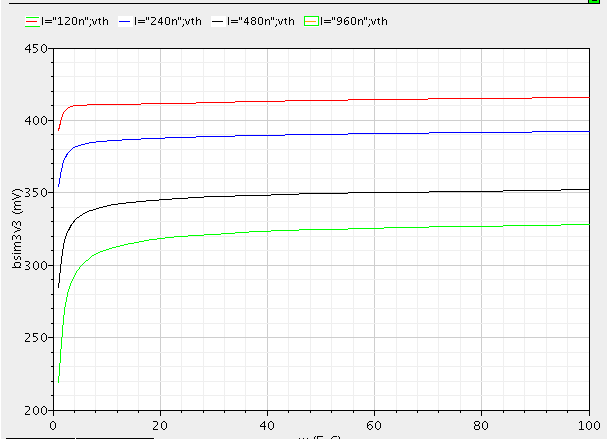
Which is similar to the obtained results in the simulation.



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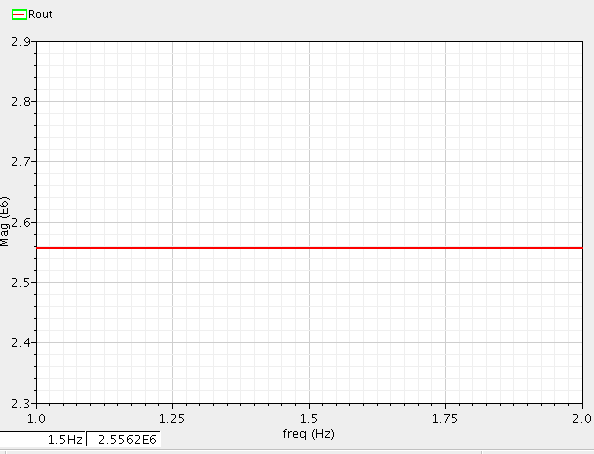
Which is similar to the obtained results of the similution.



as seen from the results that almost constant(slitly increase) with the width of the transistor and it decreases with the increase of the process technology and it increases with temprature

# Task 2:

Figure 2:DC operating point annotation with dimensions

Using AC analysis we obtained the value

Of the output resistance from frequency 1:2 Hz which is considered DC and with AC magnitude = 1 v

Figure 3:output resistance.

Which is much more the the required value in the design specifications.

From the operating point the value of which is valid by the design specifications.

# Systematic offset

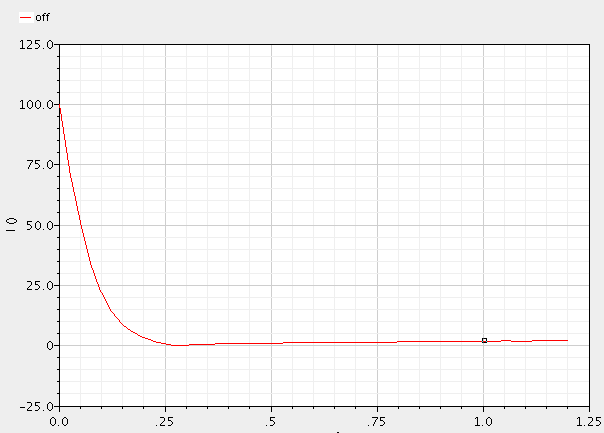


Figure :Iout with Vout from 0 to 1.2

# Observations and conclusions:

In this design we found it hard to work with as the values for was so small and the value for the was large that we couldn’t accomplish the design specifications so we used a process technology of .

For the mirroring ratio to be 1:2 , we used the widths of the transistors of the reference part of the current mirror half the width of the widths of the output part.

And after choosing the values of w3, w2 from the characteristics graphs obtained in the first task, we observed that changing the value of W2 changes the value of Vcomp as it changes the value of Vds and also changes the accuracy of the mirroring ratio.The value of the output resistance changes with the value of W3.

The systematic offset of the current mirror increases dramatically with decreasing the of it, and at approximately , it starts to saturate approaching , and although the systematic offset is very low below the achieved , the output resistance still very low compared with it’s values close to .

The results obtained from the hand analysis were not accurate and the results in the simulation were slightly different from the hand analysis as the equations we use is derived from a simplified model of the transistor, so simulating the values we obtained from the hand analysis we changed the values of the parameters of the transistor to achieve design requirements .

# Task 3:VCO

The voltage controlled oscillator is an oscillator which its output frequency is controlled with the input voltage .



Figure 5:schematic with bias current

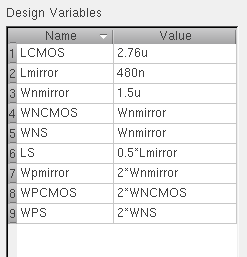
To ease modifying the dimensions of the transistors we put theme as variables and the values we used to obtain the required frequency as shown .

Figure 6:transistor parameters used in the simulation.

The bias current .

For the oscillations to start we needed to seed an initial condition for the output of the last inverter .

# The output frequency

1. the output of the last inverter with frequency .

The error = 0.126%.

# Waveforms of all inverter outputs:

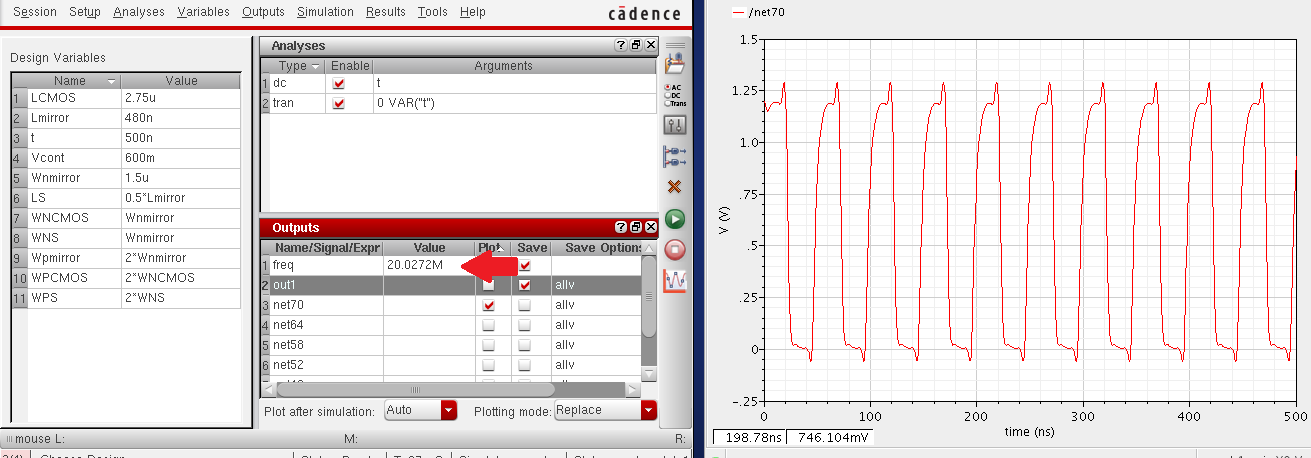
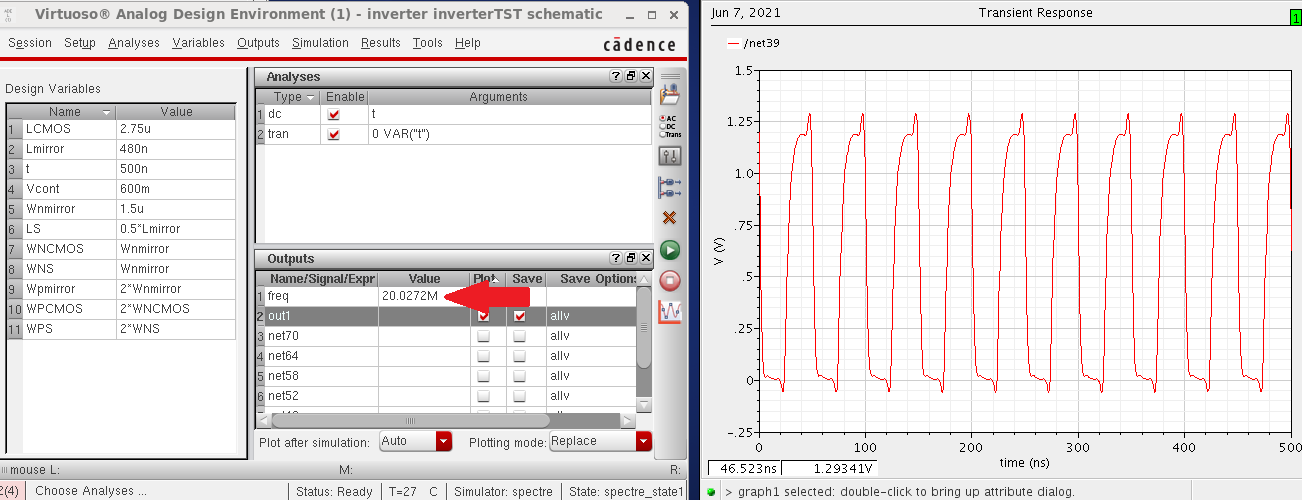


Figure :out of first inverter

Figure :output of second inverter

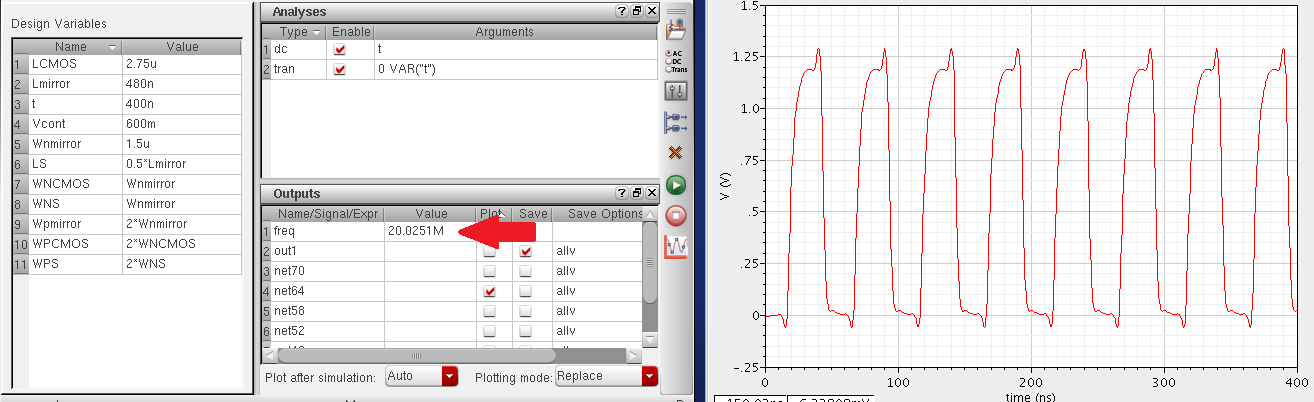


Figure :output of 3rd inverter

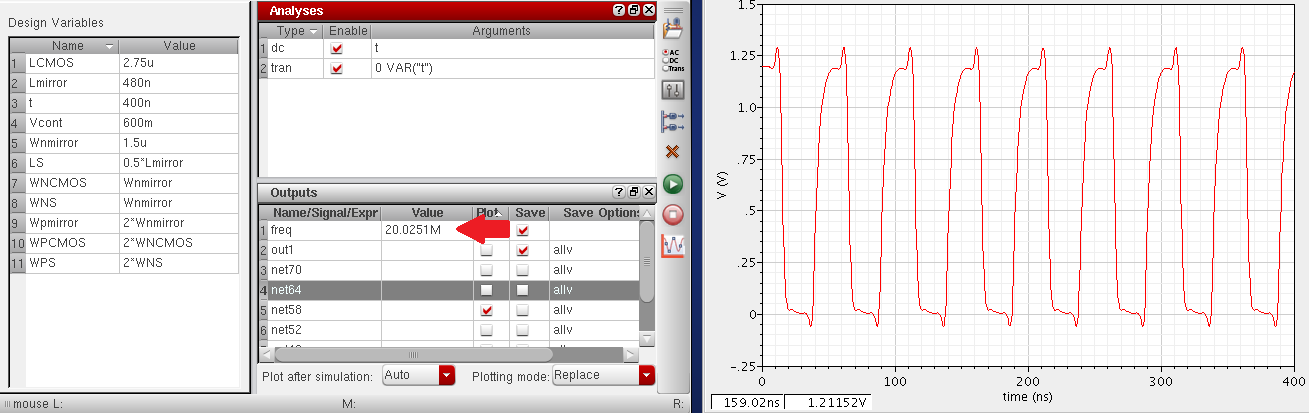


Figure :output of 4th inverter

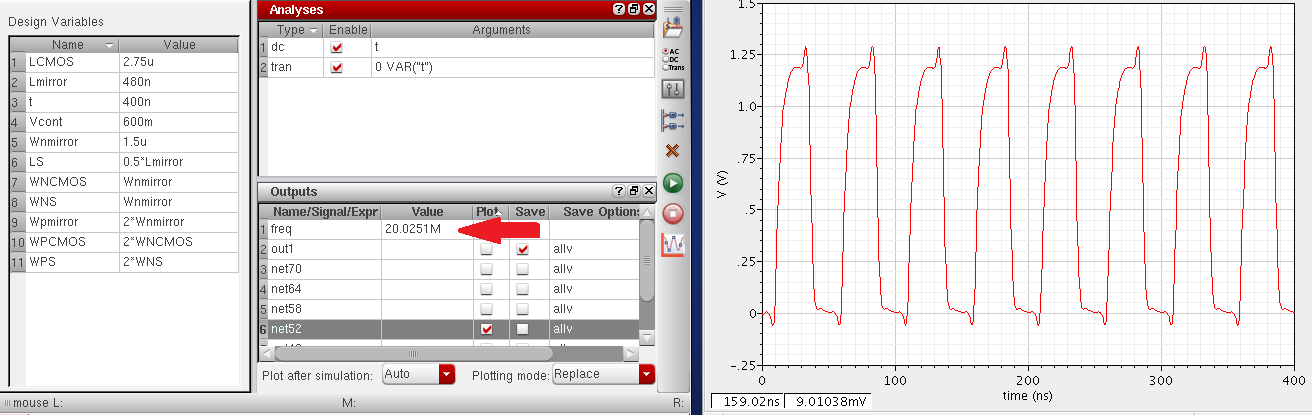


Figure :output of 5th inverter

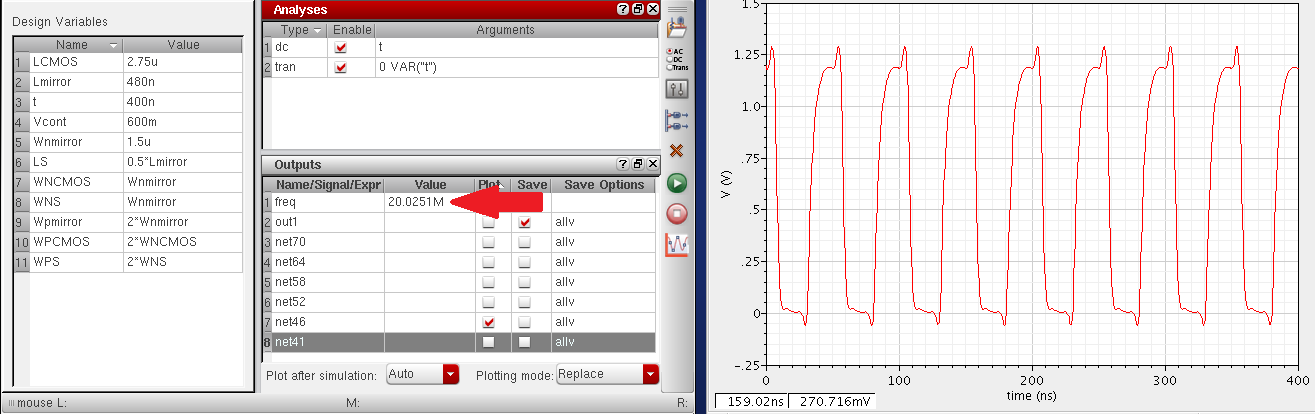


Figure :output of inveter no. 6

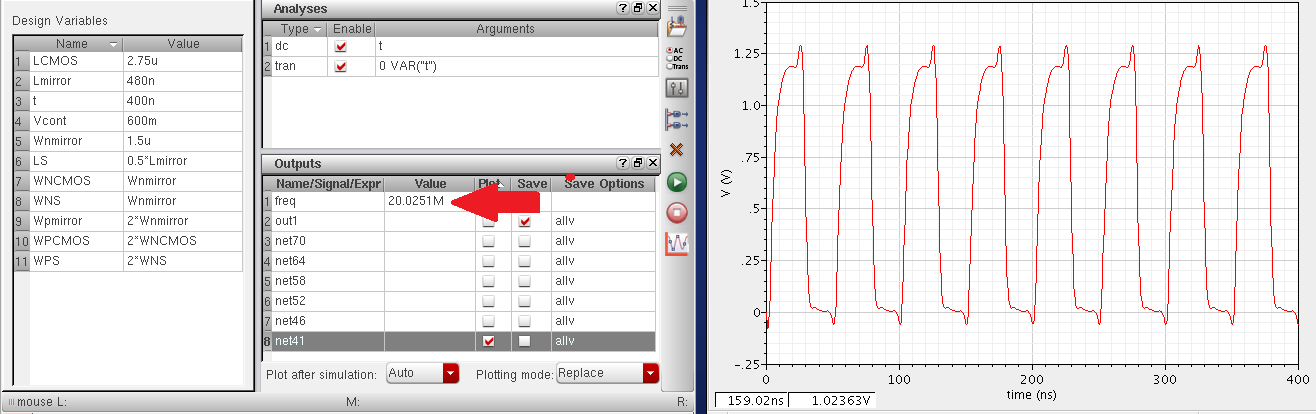


Figure :output of inverter no. 7

# Varying with frequency:

|  |  |
| --- | --- |
|  |  |
| 0 | 796.6 |
| 1.00E-01 | 1.45E+04 |
| 2.00E-01 | 2.66E+05 |
| 3.00E-01 | 2.98E+06 |
| 4.00E-01 | 1.28E+07 |
| 5.00E-01 | 1.88E+07 |
| 6.00E-01 | 2.00E+07 |
| 7.00E-01 | 2.06E+07 |
| 8.00E-01 | 2.08E+07 |
| 9.00E-01 | 2.10E+07 |
| 1.00E+00 | 2.11E+07 |
| 1.10E+00 | 2.12E+07 |
| 1.20E+00 | 2.12E+07 |

as seen from the schematic the frequency increases

with the increase in Vcont.

to plot the frequency we used the parametric analysis to swap Vcont for output expression:

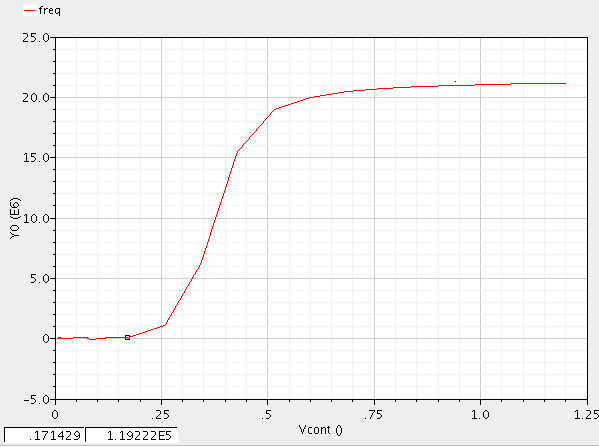
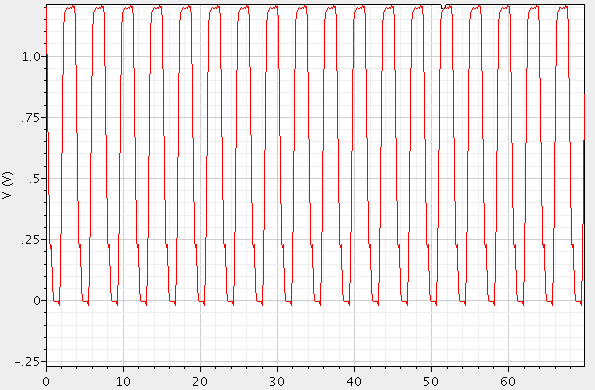
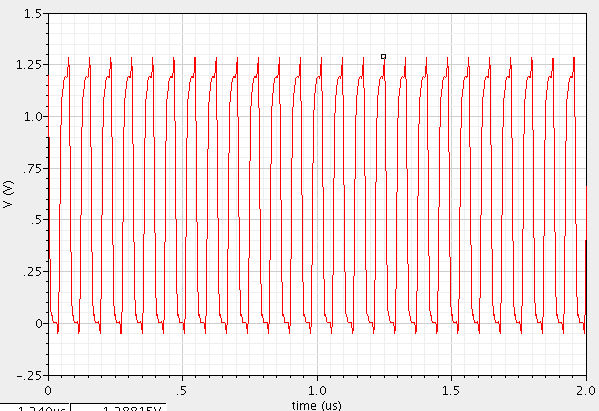
frequency(v("/net39" ?result "tran-tran"))

Figure :frequency of the ouput oscillations with the change in

# Out for three steps:



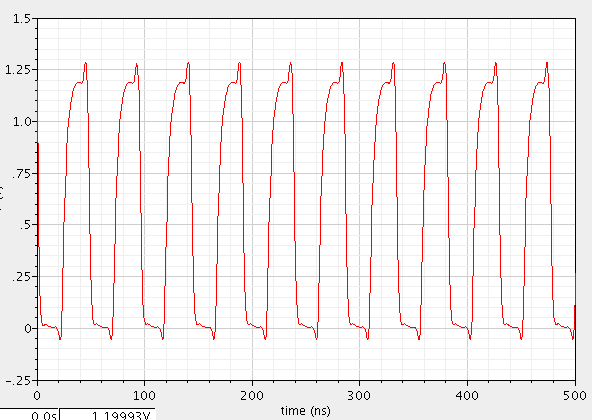


Figure 8:Vcont = 0.9v

Figure 7:Vcont = 0.4v

Figure 6:Vcont = 0.2v

# Conclusion and observations:

1. For increasing of the oscillator, the frequency of the output signal increases. It’s shown from the results that the rate of increase of the frequency is low and after approximately , the rate of increase increases dramatically, and it decreases again before reaching , and almost constant as closing to .
2. For the length of the transistors of the reference side of the current mirror, decreasing the length results in increasing the reference current significantly, which means consuming more power from the source of the circuit, and it doesn’t affect the frequency of the output signal of the oscillator.
3. For the width of the reference side of the current mirror: decreasing the width results in decreasing the reference current significantly, and have a small effect of the output frequency of the oscillator.
4. After changing each parameter and keeping others constant (L, W) of each transistor, we observed that the length of the CMOS inverter transistors has the greatest effect on the frequency of the output.